DATA SHEET

Low Power Double Data Rate 4 (LPDDR4)

version 1.0

VIP's USED

- azLPDDR4 (LPDDR4 Model)

PROTOCOLS

- LPDDR4 DRAM
- Versions: JESD209-4A, JESD209-4B

DELIVERABLES

LPDDR4 model

- Back-Back Testbench
- Exhaustive Test Suite
- User Guide

SUPPORT

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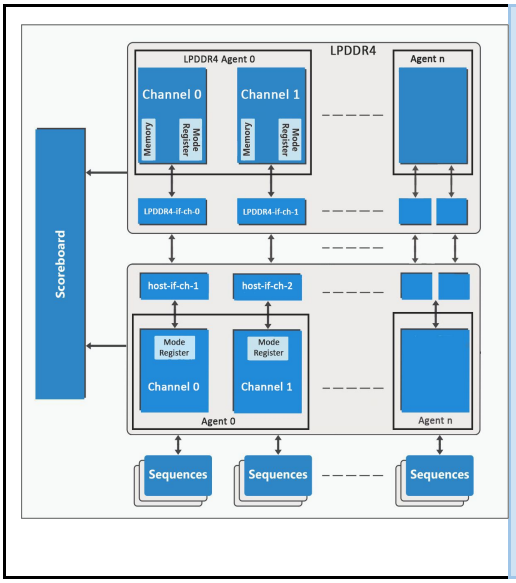

Description

The LPDDR4 solution consist of three modules (common, host, lpddr4). All three together provides a complete solution to LPDDR4 verification utility. Our UVC supports both versions (JESD209A, JESD209B) of LPDDR4. Each of the module are systemverilog model. Host is used to drive the interface signal. hbm monitors the interface signals and contributes to coverage model. common sets the both environment for host and device such as memory density, bank address size, row and column address size etc. before initiating any verification.

Features

- 16n prefetch architecture with 256 bits per memory read and write access.
- Differential clock inputs (CK_t/CK_c)
- BL = 16 and 32
- 16 DQ width
- Bank Grouping supported
- 2K or 4K Bytes per page; varies by device density/channel
- 64 bit prefetch boundary
- 2 independent channel per device.

azLPDDR4 Features

- Data mask for masking WRITE data per byte
- Self Refresh Modes
- Channel density of 4Gb to 32Gb per Die.
- DDR commands entered on each positive CK_t, CK_c edge. All other commands are one cycle command.
- Independent Command Interfaces allowing to be issued in parallel with Read/Writes in separate channels.
- 8 banks per channel; varies by device density/channel
- Auto precharge, auto refresh supported.